MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : CS-303

COMPUTER ORGANIZATION

Time Allotted: 3 Hours | *Full Marks*: 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

Group – A

(Multiple Choice Type Questions)

1. Choose the correct alternative of the following: 1×10=10

(i) The principle of locality justifies the use of

(a) Interrupt (b) Polling

(c) DMA (d) Cache memory

(ii) Instruction cycle is

(a) fetch-decode-execution (b) fetch-execution-decode

(c) decode-fetch-execution (d) decode- execution -fetch

(iii) How many RAM chips of size (256K ×1 bit) are required to build 1M Memory?

(a) 24 (b) 10

(c) 32 (d) 8

(iv) Maximum value of n bit 2's complement number is

(a) 2^n (b) $2^n - 1$

(c) $2^{n-1} - 1$ (d) Cannot be said

(v) Micro instructions are kept in

(a) Main memory (b) Control memory

(c) Cache memory (d) Secondary storage

(vi) The maximum propagation delay for *n*-bit CLA is

(a) Δ (b) Δ*n

(c) 6*Δ (d) n

(vii) The cylinder in a disk pack is

(a) collection of all tracks in a surface.

(b) logical view of same radius tracks on different surfaces of disks.

(c) collection of all sectors in a track.

(d) collection of all disks in the pack.

(viii) For which of the following multiplier numbers in Booth's algorithm maximum no. of additions and subtractions are required?

(a) 01001111 (b) 01111000

(c) 00001111 (d) 01010101

(ix) How many memory locations can be addressed by a 32-bit computer?

(a) 64 KB (b) 32 KB

(c) 4 GB (d) 4 MB

(x) The addressing mode of an instruction is resolved by

(a) ALU (b) DMA controller

(c) CU (d) program

Group – B

(Short Answer Type Questions)

Answer *any three* of the following. 5×3=15

2. Multiply decimal number (–17) and (–9) using Booth's multiplication method with step by step explanation. 5

3. Explain stack based CPU. 5

4. What is the limitation of direct-mapped cache? Explain with an example, how it can be improved into set-associative cache? 2+3=5

5. Define speedup, efficiency and throughput of a pipelined processor. Design a 4-bit Combinational circuit decrementer using four full adders. 3+2=5

6. Explain with example : Register Direct, Register Indirect and Base register addressing mode. 1½+1½+2=5

Group – C
(Long Answer Type Questions)
Answer *any three* of the following. 15×3=45

7. (a) Explain the basic block diagram of Computer System. Why do peripherals need interface circuits with them?

   (b) A block set-associative cache consists of a total of 64 blocks divided into 4 blocks sets. The main memory contains 4096 blocks, each consisting of 128 words. A block set associative cache consists of a total of 64 blocks divided into 4 blocks sets. The main memory contains 4096 blocks, each consisting of 128 words.

   (i) How many bits are there in a main memory address?

   (ii) How many bits are there in each of the TAG, SET and Word fields?

   (c) What are 'write through' and 'write back' policies in cache memory? 3+(2+5)+5=15

8. (a) Evaluate the arithmetic statement X = (A*B)/(C+D) in one, two and three address machines.

   (b) Represent the decimal value -7·5 in IEEE-754 single precision floating point format. Explain in brief about different memory access methods.

   (c) Explain Instruction Cycle with suitable flow chart. 6+(3+2)+4=15

9. (a) If a CPU has 16 bit address bus and 8 bit data bus draw the connection Diagram for this CPU with four 256 ×8 RAM and one 512 ×8 ROM.

   (b) Design a 4-bit ALU capable of performing 14 different micro operations including logical, arithmetic and shifting operations.

   (c) What is the difference between vectored and non-vectored interrupt? Average memory access time depends on which factors? 6+6+3=15

10. (a) Explain memory-hierarchy.

   (b) Can a Read Only Memory be also a Random Access Memory? Justify your answer.

   (c) Discuss the concept of associative memory unit using suitable example.

   (d) Define "latency time" in a memory. 4+2+6+3=15

11. Write short notes on *any three* of the following: 5×3=15

(a) Instruction Format

(b) Carry Look-ahead Adder

(c) Design of 4-bit ALU

(d) RISC

(e) Overflow in Fixed-point Representation
