MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : CS-303

COMPUTER ORGANIZATION

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) The main purpose for using single Bus structure is

      a) Fast data transfers

      b) Cost effective connectivity and speed

      c) Cost effective connectivity and ease of attaching peripheral devices

      d) none of these.

ii) The ALU makes use of ..... to store the intermediate results.

a) Accumulators b) Registers

c) Heap d) Stack.

iii) ..... is generally used to increase the apparent size of physical memory.

a) Secondary memory

b) Virtual memory

c) Hard disk

d) Disks.

iv) The time delay between two successive initiations of memory operation is

a) Memory access time

b) Memory search time

c) Memory cycle time

d) Instruction delay.

v) The main advantage of multiple bus organisation over single bus is

a) Reduction in the number of cycles for execution

b) Increase in size of the registers

c) Better connectivity

d) None of these.

vi) When performing a looping operation, the instruction gets stored in the

a) Registers b) Cache

c) System heap d) System stack.

vii) In case of Zero-address instruction method the operands are stored in

a) Registers b) Accumulators

c) Stack d) Cache.

viii) The addressing mode(s), which uses the PC instead of a general purpose register is

a) Indexed with offset

b) Relative

c) Direct

d) Both (a) and (c).

ix) In a normal *n*-bit adder, to find out if an overflow has occurred, we make use of

a) AND gate b) NAND gate

c) NOR gate d) XOR gate.

x) A 24 bit address generates an address space of ..... locations.

a) 1024 b) 4096

c) 2 ^ 48 d) 16,777,216.

xi) To get the physical address from the logical address generated by CPU we use

a) MAR b) MMU

c) Overlays d) TLB.

xii) During transfer of data between the processor and memory we use

a) Cache b) TLB

c) Buffers d) Registers.

xiii) The return address of the Sub-routine is pointed to by

a) IR

b) PC

c) MAR

d) Special memory registers.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. a) Briefly explain the IEEE 754 standard format for floating point number representation.

b) Represent the decimal value (–7·5) in IEEE single precision format. 3 + 2

3. Two 1024 × 4 bits RAM chips are given. Design a memory of size 2048 × 4 bits.
4. What is the difference between carry look ahead adder and ripple carry adder ? Explain the role of operating system in a computer system. 2 + 3
5. Explain Pipelining and Hazards. Define latency time of a memory. 3 + 2
6. a) What are the advantages of associative mapping over direct mapping ?
   b) Consider a series of address references given : 2, 3, 11, 16, 21, 13, 64 and 48. Assuming a direct mapped cache with 8 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the final contents of the cache. 2 + 3

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Present the Booth's algorithm for multiplication of signed 2's complement number in a flow chart and explain.
   b) Multiply (–12) and (+6), using Booth's multiplication algorithm.
   c) Divide (–15) by (–3) using Restoring & Non-restoring Division algorithm. 5 + 5 + 5

8. Discuss in detail the various factors that need to be considered while designing the ISA of a processor. Compare and contrast of RISC and CISE architecture. 10 + 5

9. Explain in detail the Bus Arbitration techniques in DMA.

10. a) Can ROM be also a RAM ? Justify your answer.
    b) What is speed up ? Prove that maximum speed up will be *K*.
    c) A disk pack has 20 surfaces. Storage area on each surface has an inner diameter of 22 cm and outer diameter of 33 cm. Maximum storage density on each track is 2000 bits/cm and maximum spacing between tracks is 0·25 mm.
        i) What is the storage capacity of the pack ?
        ii) What is the data transfer rate in bytes per second at a rotational speed of 7200 r.p.m. ?
    d) What is the necessity of Guard bits ? 3 + 3 + 6 + 3

11. a) What are the advantages of relative addressing mode over direct addressing mode ?
    b) Compare and contrast Memory mapped I/O and I/O mapped I/O.
    c) Explain the importance of a common bus system in a computer. Why I/O bus is different from a system bus ? 4 + 6 + (2 + 3)

12. Write short notes on any *three* of the following : 3 × 5

a) Addressing modes

b) Static and dynamic memory

c) Instruction pipelining

d) Concept of programmed I/O

e) Bus organization using tri-state.