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Paper Code : CS-303

COMPUTER ORGANISATION

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) RAM is called DRAM (Dynamic RAM) when

      a) it is always moving around data

      b) it requires periodic refreshing

      c) it can do several things simultaneously

      d) none of these.

   ii) Floating point representation is used to store

      a) Boolean values b) Whole numbers

      c) Real numbers d) Integers.

iii) A given memory chip has 12 address pins and 4 data pins. It has the ..... number of locations.

a) 2^4 b) 2^{12}

c) 2^{48} d) 2^{16}.

iv) In order to execute a program instructions must be transferred from memory along a bus to the CPU. If the bus has 8 data lines, at most one 8 bit byte can be transferred at a time. How many memory accesses would be needed in this case to transfer a 32 bit instruction from memory to the CPU ?

a) 1 b) 2

c) 3 d) 4.

v) A computer's memory is composed of 8K words of 32 bits each. How many bits are required for memory address if the smallest addressable memory unit is a word ?

a) 13 b) 8

c) 10 d) 6.

vi) Cache memory refers to

a) cheap memory that can be plugged into the mother board to expand main memory

b) fast memory present on the processor chip that is used to store recently accessed data

c) a reserved portion of main memory used to save important data

d) a special area of memory on the chip that is used to save frequently used data.

vii) SIMD represents an organization that

a) refers to a computer system capable of processing several programs at the same time

b) represents organization of single computer containing a control unit, processor unit and a memory unit

c) includes many processing units under the supervision of a common control unit

d) none of these.

viii) The circuit used to store one bit of data is known as

a) Register b) Encoder

c) Decoder d) Flip-flop.

ix) $(2FAOC)_{16}$ is equivalent to

a) $(195084)_{10}$

b) $(00101111101000001100)_2$

c) Both (a) and (b)

d) None of these.

x) The addressing mode used in an instruction of the form ADD X Y is

a) absolute b) indirect

c) index d) none of these.

xi) Write Through technique is used in which memory for updating the data ?

a) Virtual memory b) Main memory

c) Auxiliary memory d) Cache memory.

xii) A stack-organised computer uses instruction of

a) Indirect addressing b) Two addressing

c) Zero addressing d) Index addressing.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following $3 \times 5 = 15$

2. Explain indirect address mode. How is the effective address calculated in this case ?

3. Design a 4-bit combinational circuit decrementer using four full adders.

4. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

   i) How many selection inputs are there in each multiplexer ?

   ii) How many multiplexers are there in the bus ?

5. Write a program to evaluate the arithmetic statement $Y = (A - B + C) / (G + H) -$

   i) using an accumulator type computer with one address instruction.

   ii) using a stack organized computer with zero-address instruction.

6. Show how to implement a full adder, by using half adders..

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) A computer uses a memory unit with 256 K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts : an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part –

   i) How many bits are there in the operation code, the register code part, and the address part ?

   ii) Draw the instruction word format and indicate the number of bits in each part.

   iii) How many bits are there in the data and address inputs of the memory ?

   b) Use restoring method to divide 10100011 by 1011.

   c) Suppose we are given RAM chips each of size 256 × 4. Design a 2K × 8 RAM system using this chip as the building block. Draw a net logic diagram of your implementation. 5 + 5 + 5

8. a) For Booth's algorithm, when do worst case and best case occur ? Explain with example.

   b) What are the advantages of Interrupt I/O over Programmed I/O ?

   c) Draw the logic diagram of the cell of one word in associative memory including the read and write logic. 4 + 4 + 7

9. a) Explain the various phases of instruction cycle in a basic computer.

   b) What is Von Neumann bottleneck ? How can this be reduced ?

   c) A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from the main memory. The main memory size is 128 K × 32.

      i) How many bits are there in the tag, index block and word fields of the address format ?

      ii) What is the size of the cache memory ?

10. a) Differentiate between hardwared control and micro-programmed control. Draw the block diagram of a basic hardwared control organization with two decoders, a sequence counter and a number of control logic gates.

b) A hierarchical Three-Level Memory (Cache, Main memory, Hard Disc) system has the following specifications :

i) Cache Memory Access Time is 10nsec.

ii) Disc Access Time is 150nsec.

iii) Hit ratio of Cache Memory is 0·97

iv) Hit ratio of Main Memory is 0·9.

What should be the Main Memory access time to achieve an overall access time of 20nsec ?

c) Explain the basic DMA operations for transfer of data between memory and peripherals.

(2 + 3) + 6 + 4

11. a) What are the hazards of instruction pipelining ? How are these taken care of ?

b) Explain the Strobe Control method of Asynchronous data transfer. What are the disadvantages of this method ?

c) What do you understand by the term 'Program Interrupt' ? Explain with the help of suitable diagrams. 5 + 5 + 5